REMARKS

Present Status of the Application

The Office Action rejects claims 20-23 under 35 U.S.C. 103(a) as being unpatentable over Tao et al. (US 6,316,828) in view of Stearns et al. (US 5,895,967), and further in view of Yamaura et al. (US 6,831,360). The Office Action also indicates that the product-by-process limitation "the step of forming" has not given patentable weight.

Upon entry of the amendments in this response, claims 20 and 21 are amended. Claim 20 is amended by incorporating a feature that is supported by, for example, Figs. 2A-2B, and the specification, paragraphs [0014] and [0015]. Claim 21 is amended because of the product-by-process limitation. Hence, claims 20-23 remain pending in the present application, with claim 20 being a independent claim. Thus, reconsideration of those claims is respectfully requested.

Response to Rejection under 35 U.S.C. 103(a)

The Office Action rejects claims 20-23 under 35 U.S.C. 103(a) as being unpatentable over Tao et al. (US 6,316,828) in view of Stearns et al. (US 5,895,967), and further in view of Yamaura et al. (US 6,831,360).

The independent claim 20, as amended, recites as follows.

20. A package substrate adapted to carry a die of a wire bonding type, the package substrate at least comprising:
a substrate having a surface, a power pad, a ground pad and a signal pad, wherein the surface of the substrate having a die bonding area, the power pad, the ground pad and the signal pad disposed outside the die bonding area;
at least one passive component disposed between the power pad and the ground pad, the passive component having at least two electrodes which are connected to the power pad and the ground pad respectively; and
a metal layer simultaneously formed on exposed surfaces of the electrodes and exposed surfaces of the power pad, the ground pad and the signal pad.

(emphasis added)

Yamaura et al. disclosed, "As shown in FIG. 3(b), the connection terminal 3d for the chip part 3 comprises, for example, an AG--PD electrode 3e, and an Ni underlying plating layer 3f and a solder plating layer 3g orderly from the lower surface and the substrate terminal 4a comprises a Cu member 4c, an Ni under plating layer 4d and a gold plating layer 4b orderly from the lower layer and, further, the region of the substrate terminal 4a other than the place to form the solder connection portion 5 is covered with an overcoat glass 4e as an insulative film (solder resist film)" (col. 9 line 64- col. 10 line 6) .

According to the above mentioned, Yamaura et al. disclose that the connection terminal (3d) comprises a AG--PD electrode (3e) which should be a chip thermister (3c), an Ni underlying plating layer (3f) and a solder plating layer (3g) orderly from the lower surface. In other words, the Ni underlying plating layer (3f) and the solder plating layer (3g) are orderly formed on the chip thermister (3c). In addition, Yamaura et al. also disclose that the substrate terminal (4a) comprises a Cu member (4c), an Ni under plating layer (4d) and a gold plating layer (4b) orderly from the lower layer. In other words, the Ni under plating layer (4d) and the gold plating layer (4b) are orderly formed on the Cu member (4c).

Since the Ni underlying plating layer (3f) and the solder plating layer (3g) are formed in a process, and the Ni under plating layer (4d) and the gold plating layer (4b) are formed in another process, the Ni underlying plating layer (3f), the solder plating layer (3g), and the Ni under plating layer (4d) are not formed simultaneously, and do not connect both of the passive component electrode (3d) and the corresponding substrate pad (4a). However, Yamaura et al. do not disclose, hint or suggest the feature that "***a metal layer simultaneously formed on exposed***

surfaces of the electrodes and exposed surfaces of the power pad, the ground pad and the signal pad" defined in the independent claim 1, as amended. Therefore, even though the disclosure by Tao et al., Stearns et al., and Yamaura et al. are combined, the subject matters claimed in the present invention can not be attained.

For at least the foregoing reasons, Applicant respectfully submits that the independent claim 20 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 21-23 patently define over the prior art as well.

Application No.: 10/714,336 **Docket No.: JCLA11475**

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 20-23 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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